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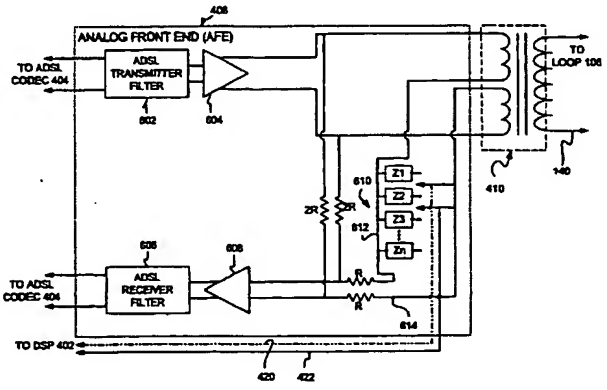
(54) Title: ACTIVE HYBRID WITH DYNAMIC IMPEDANCE MATCHING AGAINST DIFFERENT LOOP CONDITIONS AND RELATED METHOD



(57) Abstract: A system and method are disclosed for matching, or approximating, the impedance of an ADSL modem with the impedance of the associated loop by selectively switching in different impedances to improve or enhance ADSL performance in a variety of loop conditions. Using relays or multiplexers to actively switch in and out different impendance networks, the ADSL modem may select an impedance from a set of impedances (610, 612) that best matches the loop impedance. The different impedances may be switched singly or in combination with other impedances. Lastly, systems and methods are disclosed for using DSP measurement of the ADSL transmitter's (602) echo signal as the basis for determining hybrid impedance matching.

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ACTIVE HYBRID WITH DYNAMIC IMPEDANCE MATCHING AGAINST DIFFERENT LOOP CONDITIONS AND RELATED METHOD

By Ting Sun

BACKGROUND OF THE INVENTION

1. Technical Field

This invention relates generally to DSL modems and, more particularly, to a DSL modem with impedance matching capability against a variety of loop conditions and impairments.

2. Description of the Background Art

As the Internet continues to become more popular, there is an increasing need for accessing and navigating ("surfing") the Internet at high speed and at low cost. Providing high speed Internet access permits users to send and receive information over the Internet quickly and reduces the time the user must wait to receive requested information. In addition, there is a continuous pressure to lower the cost of accessing the Internet and Internet-related devices.

One method of accessing the Internet is by using Digital Subscriber Line (DSL) technology. Various versions of DSL exist, such as Asymmetric DSL (ADSL), Symmetric DSL (SDSL), Rate Adaptive DSL (RADSL), Very high speed ADSL (VADSL), Consumer DSL (CDSL), etc., and may be collectively referred to as xDSL, or DSL.

ADSL is one version of DSL technology that expands the useable bandwidth of existing copper telephone lines, delivering high-speed data communications at rates up to about 8 Mbps without interrupting normal telephone service, also known as POTS (Plain Old Telephone Service). To achieve this end, ADSL uses frequency-division multiplexing (FDM) technology to carry POTS and ADSL channels all on the same twisted-pair copper telephone line.

ADSL is a point-to-point connection in that an ADSL termination device must be present on each end of the copper circuit. Since ADSL works over copper, it is an appropriate technology for the "local loop," which comprises the copper circuits running from a local telephone switch, or central office, into virtually every home and business.

Unfortunately, however, conventional ADSL systems have been problematic for a variety of reasons. One significant limitation of conventional ADSL systems relates to the analog front end (AFE) design of the ADSL modem. In particular, to achieve good data rate transmission it is important to match the impedance of the loop with that built into the hybrid of an ADSL modem. Since the characteristic impedance of the loop frequently varies due to varying loop length, unterminated bridged taps, wire splices from different gauge wire, etc., it is difficult, if not impossible, to match such a varying impedance with a single impedance network.

For example, one conventional ADSL modem analog front end is configured as a 4-wire to 2-wire trans-hybrid design and uses a single impedance network of about 100 ohms. An analog front end using a single impedance substantially matches the loop impedance much of the time, but frequently mismatches the loop's characteristic impedance, especially when unterminated bridge taps and/or wire splices of different gauge occur. Such mismatching of impedance tends to cause poor return loss, increasing noise reflection, and transmit echo signals that affect and impair the primary modem's receive signal. In result, impedance mismatching will degrade FDM ADSL modem performance.

Accordingly, a need exists for an ADSL modem that may efficiently operate under a variety of loop impedances. An additional need exists to provide an ADSL modem analog front end that is relatively inexpensive and that minimizes echo of the transmitter signal and noise reflection at the ADSL modem – loop interface.

SUMMARY

The present system overcomes or substantially alleviates prior problems associated with operating a DSL modem in connection with an existing DSL loop. In general, the present system employs an active hybrid with dynamic impedance match capability using the combination of multiple impedance matching networks to enhance or improve DSL performance in different loop conditions. The system switches in and out different impedance networks, in parallel or in series, in conjunction with a digital signal processing (DSP) algorithm to achieve an impedance match, or approximate match, between an active hybrid DSL modem and the associated DSL loop to improve the DSL data transfer between the two under different loop conditions. The switching may be accomplished, for example, by relays (mechanical or solid state), analog switches, or analog multiplexers. The loop conditions may include loop type, loop length, and loop impairment.

Pursuant to one embodiment, an ADSL modem switches in a first impedance, probes the loop, and measures an echo signal associated with the first impedance. Next, the first impedance is switched out and a second impedance is switched in or made active. Then, the ADSL modem probes the loop and measures an echo signal associated with the second impedance. If the echo signal associated with the second impedance is weaker than that associated with the first impedance, the second impedance is made the default impedance. Otherwise, the first impedance is left as the default impedance. This process may then continue for the remainder of the available impedance networks to determine which impedance network best approximates, or yields the weakest echo signal from, the loop impedance.

Alternatively, a predetermined echo threshold defines an acceptable amount of echo signal that can be tolerated and still permit acceptable ADSL performance (data connect rate). The ADSL modem then switches in and tests different impedance networks until identifying an impedance network that yields an echo signal that is less than or equal to the predetermined echo threshold. Under this approach, the ADSL modem may not have to test each of the impedance networks. Instead, the ADSL modem continues to test impedance networks until it identifies an impedance network that yields an impedance that yields less than or equal to the predetermined echo threshold.

According to another embodiment, if none of the impedance networks yields an echo signal that is less than or equal to the threshold echo signal, the process continues to determine which impedance network yields the lowest echo signal.

In one configuration, the present system employs relays, analog switches, or analog multiplexers to actively switch in and switch out different impedance networks singly, in combinations, or both. This is done in conjunction with a DSP algorithm for echo signal measurement of the local transmit signal, optimized so that the best matching impedance network can be selected to maximize first-order hybrid rejection. Maximizing the first-order hybrid rejection minimizes the amount of echo signal as well as noise reflection from the transmit path and, thus, improves or enhances ADSL performance.

Advantageously, the different impedances are complex impedances, which have different real and imaginary components to better match the impedance of the loop, which typically will include an impedance characterized by having both real and imaginary components. That is, the different impedances preferably have different real components and different complex components, which may include a capacitance or an inductance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating an ADSL service network;

FIG. 2 is a block diagram of the splitter of FIG. 1;

FIG. 3 is a block diagram illustrating an alternative ADSL service network;

FIG. 4 is a block diagram of the ADSL modem illustrated in FIGS. 1 and 3;

FIG. 5 is a block diagram of the ADSL codec illustrated in FIG. 4;

FIG. 6 is a block diagram of the Analog Front End (AFE) of FIG. 4;

FIG. 7A illustrates an example of different impedance networks associated with the different impedances shown in FIG. 6;

FIG. 7B illustrates another example of different impedances that may be selectively activated to match a loop impedance;

FIG. 8 is a flowchart illustrating one embodiment of a method of the present system;

FIG. 9 is a flowchart illustrating another embodiment of the method of the present system; and

FIG. 10 is a flowchart illustrating yet another embodiment of the method of the present system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates an ADSL service network 100 that includes a central office 102 including a Digital Subscriber Line Access Muliplexer (DSLAM) 103 and a home 104 coupled by a loop 106. As shown, the central office 102 includes an ADSL transceiver unit 110 and a loop interface 112. The loop interface 112 includes a high pass filter 114 and a low pass filter 116 to split high frequency ADSL components of the loop signal and the lower frequency POTS (Plain Old Telephone Service) components of the loop signal. In this configuration, the high pass filter 114 passes signals in the ADSL frequency range to the broadband network 120 via the ADSL transceiver 110. Likewise, the low pass filter 116 passes the lower frequency POTS signals to the narrow band network 122 over a PSTN (Public Switched Telephone Network) line.

The home 104 is shown as including a splitter 130, an ADSL modem 132, a computer 134, a telephone, or POTS, network 136, and POTS devices, such as telephones 138. While the ADSL modem 132 is illustrated as being disposed outside of the computer 134, those skilled in the art will appreciate that the ADSL modem 132 could also be positioned inside the computer 134.

The splitter 130 splits the incoming signal into high and low frequency components. As discussed in more detail below with reference to FIG. 2, the splitter 130 routes the high frequency component along line 140 to the ADSL modem 132, which is coupled to a network device, such as a computer 134, by a line 142. Likewise, the splitter 130 routes the low frequency, or POTS, component of the incoming signal to the telephone network 136 along line 144. The telephones 138, as well as other POTS devices (*e.g.* 56k modems, facsimile machines, etc.), are coupled to the telephone network 136 by lines 148.

Additional details concerning conventional ADSL equipment are found in Standards Project for Interfaces Relating to Carrier to Customer Connection of Asymmetrical Digital Subscriber Line (ADSL) Equipment, T1E1.4/97-007R6, T1.413 Issue 2, edited by John Bingham and Frank van der Putten, dated September 26, 1997, which is incorporated herein by reference.

FIG. 2 illustrates details of the splitter 130 of FIG. 1. As shown, the splitter 130 includes a high pass filter 202 and a low pass filter 204 coupled to the loop 106 via lines 206 and 208 respectively. The high pass filter 202 permits higher frequency signals, such as ADSL signals, to pass from the loop 106 to the ADSL modem 132 (FIG. 1) while preventing the lower frequency POTS signals from entering onto the line 140 and potentially interfering with the operation of the ADSL modem 132. Similarly, the low pass filter 204 permits the lower frequency POTS signals to pass onto the telephone network 136 while preventing higher frequency signals, such as ADSL signals, from entering onto the telephone network 136 and potentially interfering with the operation of POTS devices, such as the telephones 138, coupled thereto. In addition, the low pass filter 204 isolates impedance changes on the telephone network 136 caused by the POTS devices, such as the telephones 138, such that the impedance changes do not affect the performance of the ADSL modem 132.

FIG. 3 illustrates an alternative ADSL network 300. The network 300 differs from that illustrated in FIG. 1 in that it does not include the splitter 130 disposed between the loop 106 and the telephone network 136 or the ADSL modem 132. As such, the loop 106 is directly coupled to the telephone network 136. In contrast with the network 100 shown in FIG. 1, the network 300 includes low pass filters 302 disposed between the telephones 138 and the telephone network 136. The low pass filters 302 generally prevent the higher frequency signals from interfering with operation of the telephone 138 and separate the lower frequency voice band signals from the ADSL spectrum. In addition, the low pass filters 302 isolate impedance changes on the telephone network 136 caused by the POTS devices, such as the telephones 138, such that the impedance changes do not affect the performance of the ADSL modem 132.

FIG. 4 illustrates details of the ADSL modem 132 depicted in FIGS. 1 and 3. As shown, the ADSL modem 132 includes a Digital Signal Processor (DSP) 402, an ADSL coder/decoder (codec) 404, and an Analog Front End (AFE) 406. The AFE 406 is coupled to the line 140, which leads to the loop 106 by a transformer 410. The DSP 402 is illustrated as including a PCI (Peripheral Component Interconnect) bus controller 412, which controls communications between the ADSL modem 132 and the PCI bus 414 of the computer 134 along line 416. Again, those skilled in the art will appreciate that the ADSL modem 132 can be positioned internal or external of the computer 134 and the data

peripheral interface between the computer 134 and the associated ADSL modem 132 can be, for example, Universal Serial Bus (USB) or parallel port. First and second control lines 420 and 422 interconnect the AFE 406 and the DSP 402 to enable direct communication therebetween. A central processor (not shown) may alternatively control the AFE 406.

FIG. 5 illustrates details of the ADSL codec 404 depicted in FIG. 4. The ADSL codec 404 includes a digital to analog converter 502 coupled to a reconstruction filter and attenuator 504 for converting the DSP 402 output to an analog signal and reconstructing the same. Additionally, the ADSL codec 404 includes an analog to digital signal converter 506 and a programmable gain amplifier 508 for converting to digital format the signals received by the ADSL codec 404 from the Analog Front End (AFE) 406. Accordingly, in this configuration, the ADSL codec 404 provides A/D and D/A signal conversions between the DSP 402 and the analog front end (AFE) 406.

FIG. 6 illustrates details of the Analog Front End (AFE) 406 of FIG. 4. As shown, the AFE 406 is interposed between the loop 106 and the ADSL codec 404 and includes an ADSL transmitter filter 602, an ADSL line driver with gain stage 604, an ADSL receiver filter 606, and an ADSL high-speed differential receiver 608. The ADSL transmitter filter 602 advantageously comprises a low pass filter and the ADSL receiver filter 606 advantageously comprises a band-pass filter for echo suppression and anti-aliasing. Moreover, the ADSL transmitter 604 has a gain = n1 while the ADSL high-speed differential receiver 608 has a gain = n2.

The Analog Front End (AFE) 406 also includes a set of impedance networks 610 comprising impedance networks Z1, Z2, Z3...Zn for selectively and actively changing the hybrid matching impedance of the AFE 406 to more adaptively and closely match, or approximate, the impedance of the loop 106 to improve or enhance ADSL performance. The set of impedance networks 610 are disposed between lines 612 and 614. As discussed in more detail below, relays, analog switches, or analog multiplexors (not shown) selectively switch in, or turn on, the different impedance networks. Networks Z1-Zn are switched in, or turned on, singly or in combinations to more closely match the impedance of the loop 106. In one embodiment, the different impedance networks Z1-Zn are switched in, or turned on, singly or with multiple impedance networks in parallel.

The DSP 402 (FIG. 4) may select a particular impedance or combination of impedances based on which impedance or combination of impedances yields the smallest echo signal, based on which impedance or combination of impedances yields an echo signal that is within a predetermined threshold echo tolerance, or both. The DSP 402 controls the switching of impedances Z1 – Zn via the control lines 420 and 422.

FIG. 7A illustrates one embodiment of a set of impedance networks 610 including impedances Z1 – Zn, which may be arranged in parallel or in series with each other, each impedance Z1 – Zn also having an associated switch 702. In this configuration, the impedances Z1 – Zn may be switched on singly or multiple impedances may be switched on by operation of the switches 702. As shown, the impedance networks Z1- Zn may include resistors, inductors, and capacitors. While different numbers of impedances Z1 – Zn may be employed, two or three impedances may provide a sufficient number of impedances to substantially match a very high percentage of, if not all, anticipated loop conditions at relatively low cost.

FIG. 7B depicts another set of impedance networks 720. This embodiment includes a resistor 722, a first capacitor 724, a resistor 726, a switch 728, and a second capacitor 730. As shown, the first capacitor 724 and the resistor 726 are arranged in parallel and may be selectively switched in by operation of the switch 728. Hence, this embodiment provides the selection of two different effective impedances, one impedance with the switch 728 open and another impedance with the switch 728 closed. In some applications, two impedances may be sufficient to acceptably match the impedance of the loop 106.

FIG. 8 is a flowchart 800 that depicts operation of one embodiment of the present system. Initially, as shown in block 802, the ADSL modem 132 (FIG. 4) is reset. Next, the ADSL modem 132 is powered up and the DSP 402 is initialized pursuant to block 804. The DSP 402 then sets or assigns one of the impedance networks Z1 – Zn, or a combination of impedance networks, to be the default impedance Z_0 pursuant to block 806.

Then, pursuant to block 808, the ADSL modem 132 (FIG. 4) probes the loop 106 and then measures an echo signal E_0 reflected back from the loop 106. One way in which the ADSL modem 132 may probe the loop 106 is by emitting a transmitter tone, or

multiple tones, in the ADSL signal band. The reflected echo signal may then be detected by the ADSL receiver filter 606 (FIG. 6) and the DSP 402 (FIG 4). The better the impedance match between the ADSL modem 406 and the loop 106, the weaker, or smaller, the echo signal will be. Conversely, the worse the impedance match between the ADSL modem 406 and the loop 106, the stronger, or larger, the echo signal will be.

After E_0 has been determined as described above, Z_0 is turned off, or switched out, and Z_{New} is turned on, or switched in, so that Z_{New} is the currently active impedance pursuant to block 810. Z_{New} is the next impedance to be tested. Then, in a manner similar to block 808, the ADSL modem 132 probes the loop 106 and measures the echo signal associated with Z_{New}, which is E_{New}, pursuant to block 812.

Once E_0 and E_{New} have been determined, the DSP 402 determines whether E_{New} is less than E_0 pursuant to block 814. In essence, the DSP 402 is determining whether Z_{New} results in a lower echo signal, and thus a better impedance match, than Z_0. If E_{New} is less than E_0, then execution proceeds to block 816 and Z_0 is assigned to be equal to Z_{New} and E_0 is assigned to be equal to E_{New} so that Z_{New} is the new default impedance, else execution proceeds to block 812. At block 818, the DSP 402 determines whether all of the available impedances Z1 – Zn have been checked. If there are impedances, or combinations of impedances, that have not yet been checked, then execution returns to block 810 so that the next impedance may be checked to determine whether it is a better impedance match than Z_0.

After all of the different impedances and combinations of impedances have been checked pursuant to blocks 810 – 816, the impedance with the best impedance match with the loop 106 will be Z_0. Thus, upon termination at block 820, the optimal impedance match $Z_{Optimized}$ will be equal to or the same as Z_0.

A significant advantage of employing the method of the flowchart 800 is that the best available impedance match may be determined by testing each impedance and combination of impedances. However, this method may continue to test additional impedances or combinations of impedances after an acceptable impedance has already been tested.

As another embodiment, FIG. 9 illustrates a flowchart 900 for identifying an impedance or combination of impedances that provide an acceptable impedance match with the loop 106 (FIG 1). Initially, the ADSL modem 132 (FIG. 4) is reset pursuant to block 902. Then, the ADSL modem is powered up and the DSP 402 (FIG. 4) is initialized

pursuant to block 904. Next, one of the impedances, Z1 is selected as the default impedance Z_0 pursuant to block 906. In one embodiment, the default impedance Z1 has an impedance of about 100 ohms or an impedance that is acceptable for the most common loop impedances. Once the ADSL modem 132 is thus set up, the echo threshold E_0 is set pursuant to block 908. E_0 is a predetermined echo signal magnitude that represents an acceptable echo signal threshold so that any impedance producing an associated echo signal that is equal to or less than E_0 is an acceptable impedance match with the loop 106.

Then, a first impedance, Z_N, is turned on or switched in so as to be the active impedance of the AFE 406 pursuant to block 910. The ADSL modem 132 then probes the loop 106 and measures the reflected echo signal E_N associated with the first impedance Z_N pursuant to block 912. Once the echo signal E_N has been determined, the DSP 402 compares the echo threshold E_0 with the measured echo signal E_N to determine whether the difference between E_0 and E_N is greater than or equal to zero pursuant to block 914.

In other words, the action of block 914 determines whether the measured echo signal E_N associated with the impedance Z_N is less than or equal to the echo threshold E_0 and thus represents an acceptable impedance match. If so, then execution proceeds to block 916 where the process terminates with $Z_{Optimized} = Z_0$. If not, then execution proceeds to block 918.

At block 918, Z_N is turned off, or switched out and the next impedance, Z_{N+1}, is turned on and made the new default impedance Z_0. Then, the DSP 402 determines whether this newly turned on impedance, Z_{N+1}, is the last impedance to be checked, pursuant to block 920. That is, the DSP 402 determines whether there are any more impedances Z1 – Zn to be checked. If the impedance Z_{N+1} is the last impedance to be checked, then execution continues to block 922 and Z_0 is assigned to be equal to the first impedance Z1, which, as discussed above, is chosen as a good impedance match with the most common loop characteristic impedance. Preferably, however, one of the tested impedances will have an associated echo signal that is less than or equal to the echo threshold E_0. If the determination of block 920 is "no," then execution continues to block 912 so that the newly switched in impedance may be tested to see if it yields an echo signal that is less than or equal to the echo threshold E_0.

FIG. 10 is a flowchart 1000 that depicts yet another embodiment of a method for matching the impedance of the ADSL modem 132 with the loop 106. As described below, the flowchart 1000 combines aspects of the flowcharts 800 and 900 described above with reference to FIGS. 8 and 9 respectively.

Initially, the ADSL modem 132 (FIG. 4) is reset pursuant to block 1002. Then, the ADSL modem is powered up and the DSP 402 (FIG. 4) is initialized pursuant to block 1004. Next, one of the impedances, Z_N is selected as the default impedance Z_0 pursuant to block 1006. Once the ADSL modem 132 is thus set up, the echo threshold E_0 is set pursuant to block 1008. As discussed above, E_0 is a predetermined echo signal magnitude that represents an acceptable echo signal threshold so that any impedance having an associated echo signal that is equal to or less than E_0 is an acceptable impedance match with the loop 106.

Then, a first impedance, Z_N, is turned on or switched in so as to be the active impedance of the AFE 406 pursuant to block 1010. The ADSL modem 132 then probes the loop 106 and measures the reflected echo signal E_N associated with the first impedance Z_N pursuant to block 1012. Once the echo signal E_N has been determined, the DSP 402 compares the echo threshold E_0 with the measured echo signal E_N to determine whether the difference between E_0 and E_N is greater than or equal to zero pursuant to block 1014. In other words, the action of block 1014 determines whether the measured echo signal E_N associated with Z_N is less than or equal to the echo threshold E_0 and thus represents an acceptable impedance match. If so, then execution proceeds to block 1016 where the process terminates with $Z_{Optimized} = Z_0$. If not, execution proceeds to block 1018.

At block 1018, Z_N is turned off, or switched out and the next impedance, Z_{N+1}, is turned on and made the new default impedance Z_0. Then, the DSP 402 determines whether this newly turned on impedance, Z_{N+1}, is the last impedance to be checked, pursuant to block 1020. That is, the DSP 402 determines whether there are any more impedances Z1 – Zn to be checked. If the impedance Z_{N+1} is the last impedance to be checked, then execution continues to block 1020, which directs execution to block 806 of the flowchart 800 shown in FIG. 8 and described above so that the best impedance match of the available impedances may be employed. If the determination of block 1020 is "no," then execution continues to block 1012 so that the newly switched in impedance may be tested to see if it yields an echo signal that is less than or equal to the echo threshold E_0.

The invention has been described above with reference to specific embodiments. It will, however, be evident that various modifications and changes may be made thereto

without departing from the broader spirit and scope of the invention as set forth in the appended claims. The foregoing description and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A modem for interfacing a computer and a loop, the loop having a loop impedance, the modem comprising:

an analog front end having multiple impedance networks for actively providing an impedance value that approximates the loop impedance; and

a digital signal processor configured to control activation of the multiple impedance networks.

2. The modem of claim 1, wherein the analog front end in conjunction with the digital signal processor tests each of the impedance networks to determine which one of the impedance networks approximates the loop impedance.

3. The modem of claim 2, wherein the analog front end tests at least one of the impedance networks by measuring an echo signal corresponding to the tested impedance network.

4. The modem of claim 3, wherein the digital signal processor compares the echo signal corresponding to at least one of the impedance networks to an echo threshold value to identify one of the impedance networks that acceptably approximates the loop impedance.

5. The modem of claim 4, wherein the impedance network that corresponds to an echo signal less than or equal to the echo threshold value is the impedance network that approximates the loop impedance.

6. The modem of claim 3, wherein the digital signal processor identifies which of the impedance networks yields a minimum echo signal, and employs the identified impedance network to approximate the loop impedance.

7. The modem of claim 3, wherein the digital signal processor compares the echo signal corresponding to each tested impedance network to an echo threshold value, determines whether the corresponding echo signal is less than or equal to the echo threshold value, and if none of the tested impedance networks corresponds to an echo signal that is less than or equal to the echo threshold value, the processor selects the impedance network corresponding to the weakest echo signal.

8. The modem of claim 1, wherein the impedance networks are connected in parallel.

9. The modem of claim 1, wherein the impedance networks are connected in series.

10. The modem of claim 1, wherein the impedance networks are complex impedances including capacitance values.

11. The modem of claim 1, wherein the impedance networks are complex impedances including inductance values.

12. The modem of claim 1, wherein the impedance networks are complex impedances including capacitance values and inductance values.

13. The modem of claim 1 being an Asymmetric Digital Subscriber Line (ADSL) modem.

14. The modem of claim 1, wherein the analog front end in conjunction with the digital signal processor tests combinations of the impedance networks to determine a combination of the impedance networks that approximates the loop impedance.

15. A method for approximating a loop impedance of a loop, comprising the steps of:
providing a set of impedance networks;
measuring an echo signal corresponding to each of the impedance networks; and
determining which one of the impedance networks approximates the loop impedance using the echo signals corresponding to the impedance networks.

16. The method of claim 15, wherein the step of determining which one of the impedance networks approximates the loop impedance includes comparing the echo signal corresponding to each of the impedance networks to an echo threshold value, wherein a measured echo signal that is less than or equal to the echo threshold value corresponds to the impedance network that approximates the loop impedance.

17. The method of claim 15, wherein the step of determining which one of the impedance networks approximates the loop impedance further comprises determining a minimum echo signal of the echo signals corresponding to the impedance networks such that the minimum echo signal corresponds to the impedance network that approximates the loop impedance.

18. The method of claim 15, wherein the step of determining which one of the impedance networks approximates the loop impedance further comprises comparing the echo signal corresponding to each of the impedance networks to an echo threshold value, wherein an echo signal that is less than or equal to the echo threshold value corresponds to the impedance network that approximates the loop impedance, and if no echo signal is less than or equal to the echo threshold value, determining a minimum echo signal such that the minimum echo signal corresponds to the impedance network that approximates the loop impedance.

19. The method of claim 15, wherein the set of impedance networks includes complex impedances.

20. The method of claim 15 implemented in a modem for interfacing a computer to the loop.

21. The method of claim 20 wherein the modem is an Asymmetric Digital Subscriber Line (ADSL) modem.

22. A device for approximating an unknown impedance of a system, the device comprising:

a plurality of impedance networks, each impedance network having an impedance value;

a switching mechanism for selectively activating at least one of the impedance networks; and

a processor configured to control the switching mechanism to select an impedance network that approximates the unknown impedance.

23. The device of claim 22, wherein the processor is configured to select the impedance network that approximates the unknown impedance by testing each of the impedance networks, and selecting the impedance network that best approximates the unknown impedance.

24. The device of claim 22, wherein the processor is configured to select the impedance network that approximates the unknown impedance by measuring an echo signal that corresponds to each impedance network, and selecting the impedance network that best approximates the unknown impedance.

25. The device of claim 22, wherein the switching mechanism is implemented as a relay.

26. The device of claim 22, wherein the switching mechanism is implemented as an analog multiplexer.

27. The device of claim 22, wherein the processor is a digital signal processor and the impedance values are complex impedances.

28. The device of claim 27, wherein the complex impedances include capacitance values.

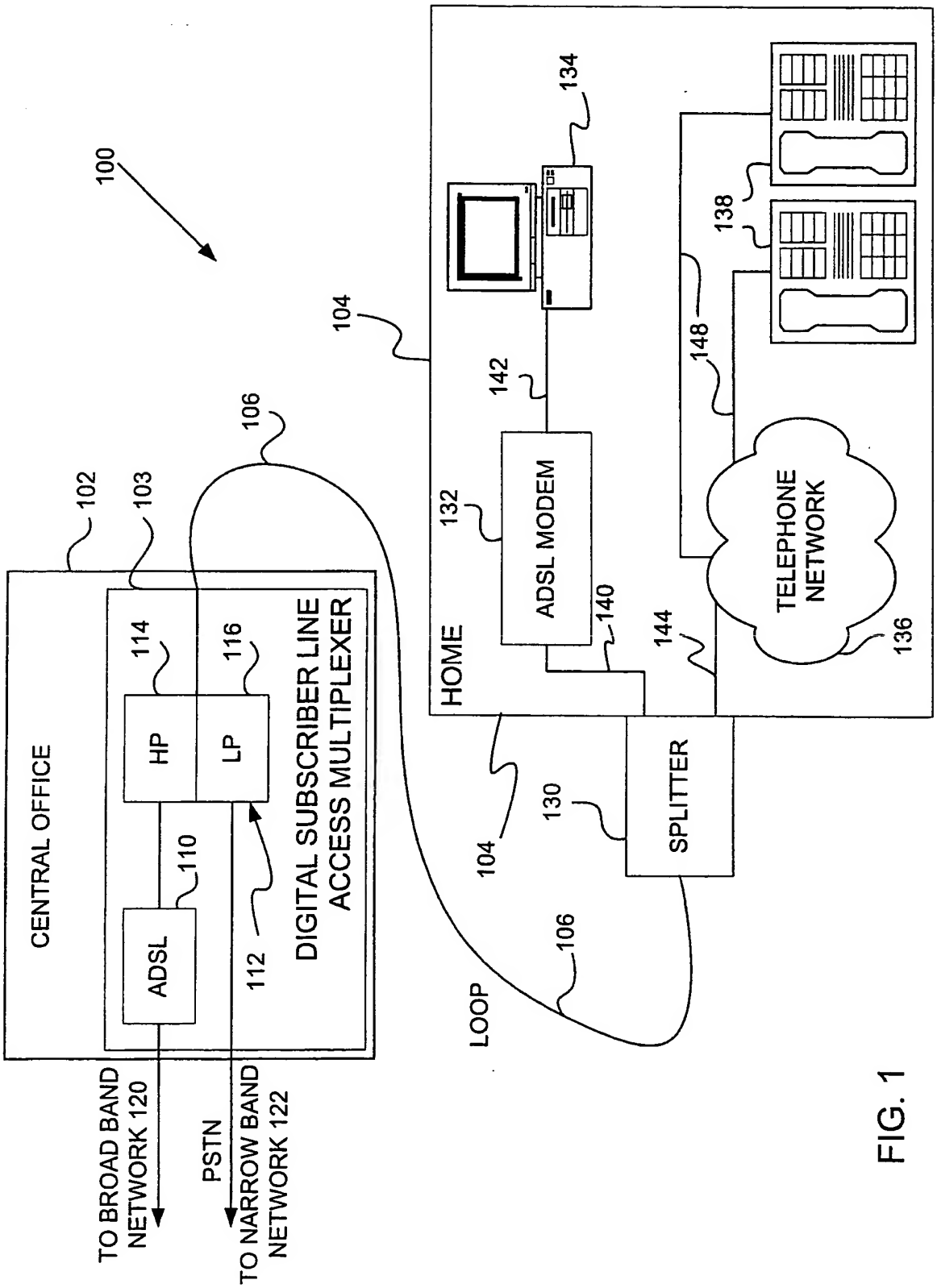
29. The device of claim 27, wherein the complex impedances include inductance values.

30. A device for substantially matching an unknown impedance, comprising:

a set of impedance network means;

means for measuring an echo signal corresponding to each of the impedance network means; and

means for determining which one of the impedance network means substantially matches the unknown impedance using the echo signals corresponding to the impedance network means.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CENTRAL OFFICE
102
103
DIGITAL SUBSCRIBER LINE ACCESS MULTIPLEXER
HP
LP
114
116
ADSL
110
112
106
TO BROAD BAND NETWORK 120
PSTN
TO NARROW BAND NETWORK 122
LOOP
104
130
SPLITTER
144
HOME
132
ADSL MODEM
140
142
134
104
148
138
TELEPHONE NETWORK
136

FIG. 1

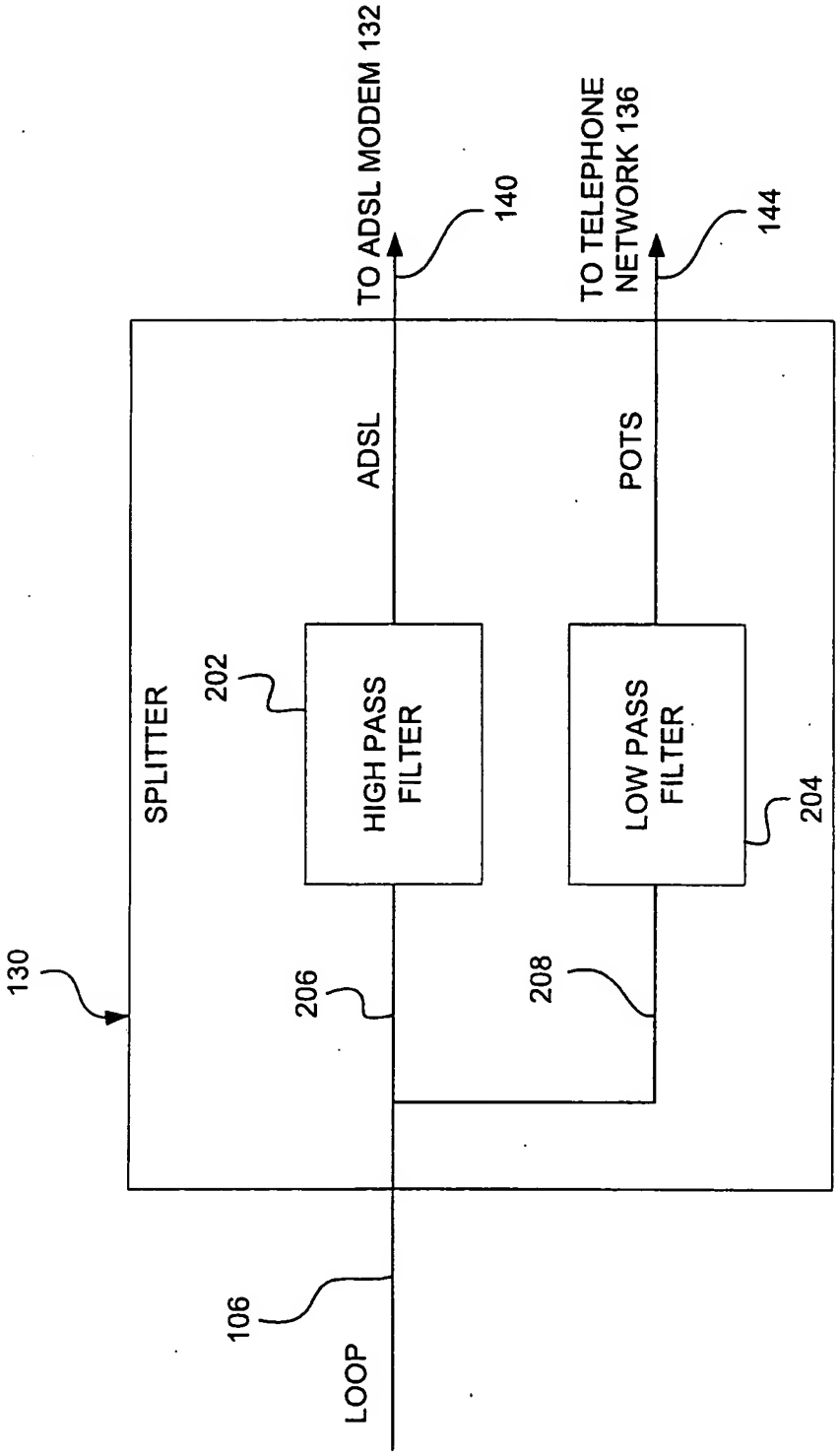
TO ADSL MODEM 132
140
TO TELEPHONE NETWORK 136
144
ADSL
POTS
SPLITTER
202
HIGH PASS FILTER
LOW PASS FILTER
204
130
206
208
106
LOOP

FIG. 2

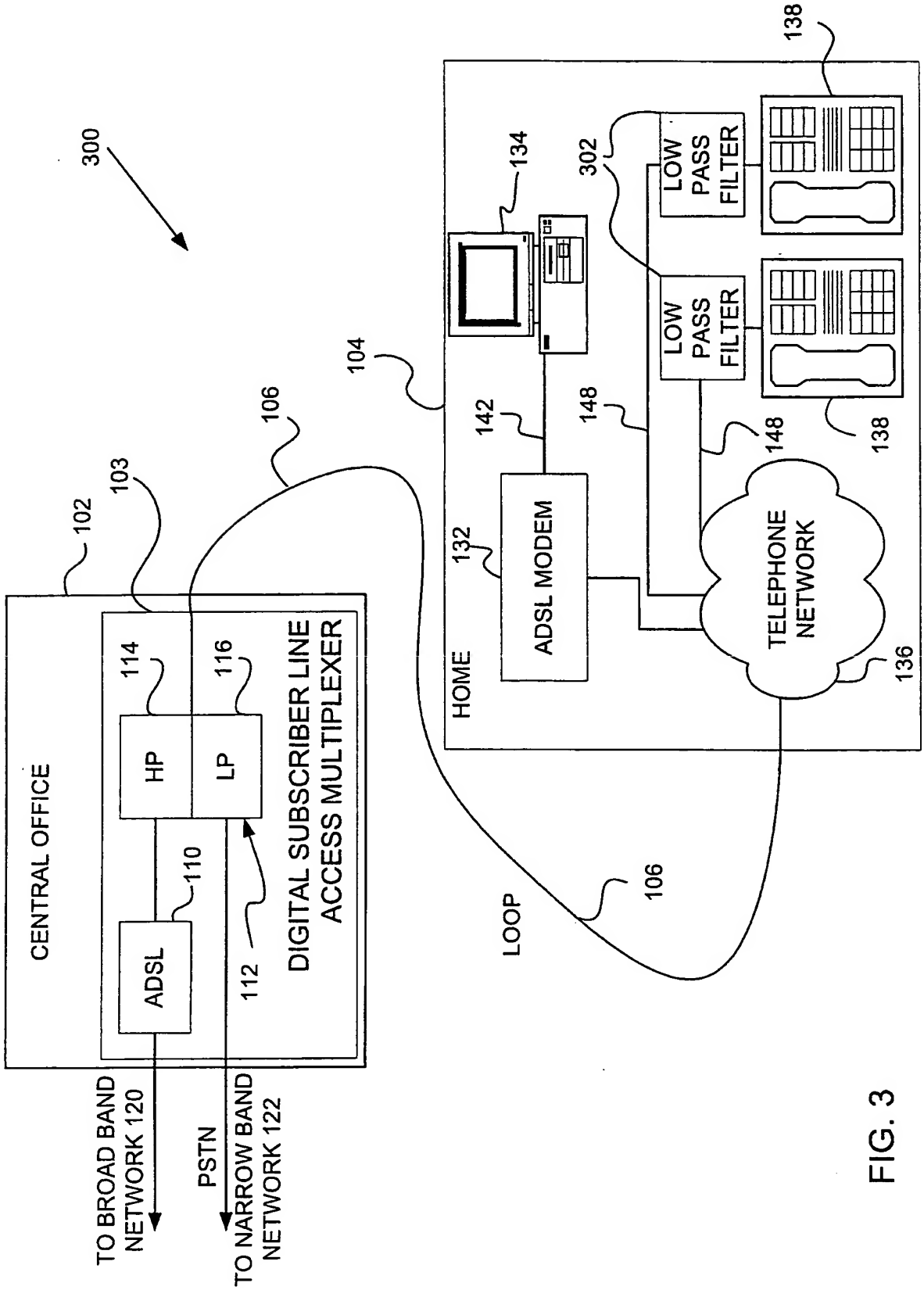
300
CENTRAL OFFICE
102
103
DIGITAL SUBSCRIBER LINE ACCESS MULTIPLEXER
HP
LP
ADSL
110
112
114
116
106
104
LOOP
106
HOME
ADSL MODEM
132
142
134
148
148
TELEPHONE NETWORK
136
LOW PASS FILTER
LOW PASS FILTER
302
138
138
TO BROAD BAND NETWORK 120
PSTN
TO NARROW BAND NETWORK 122

FIG. 3

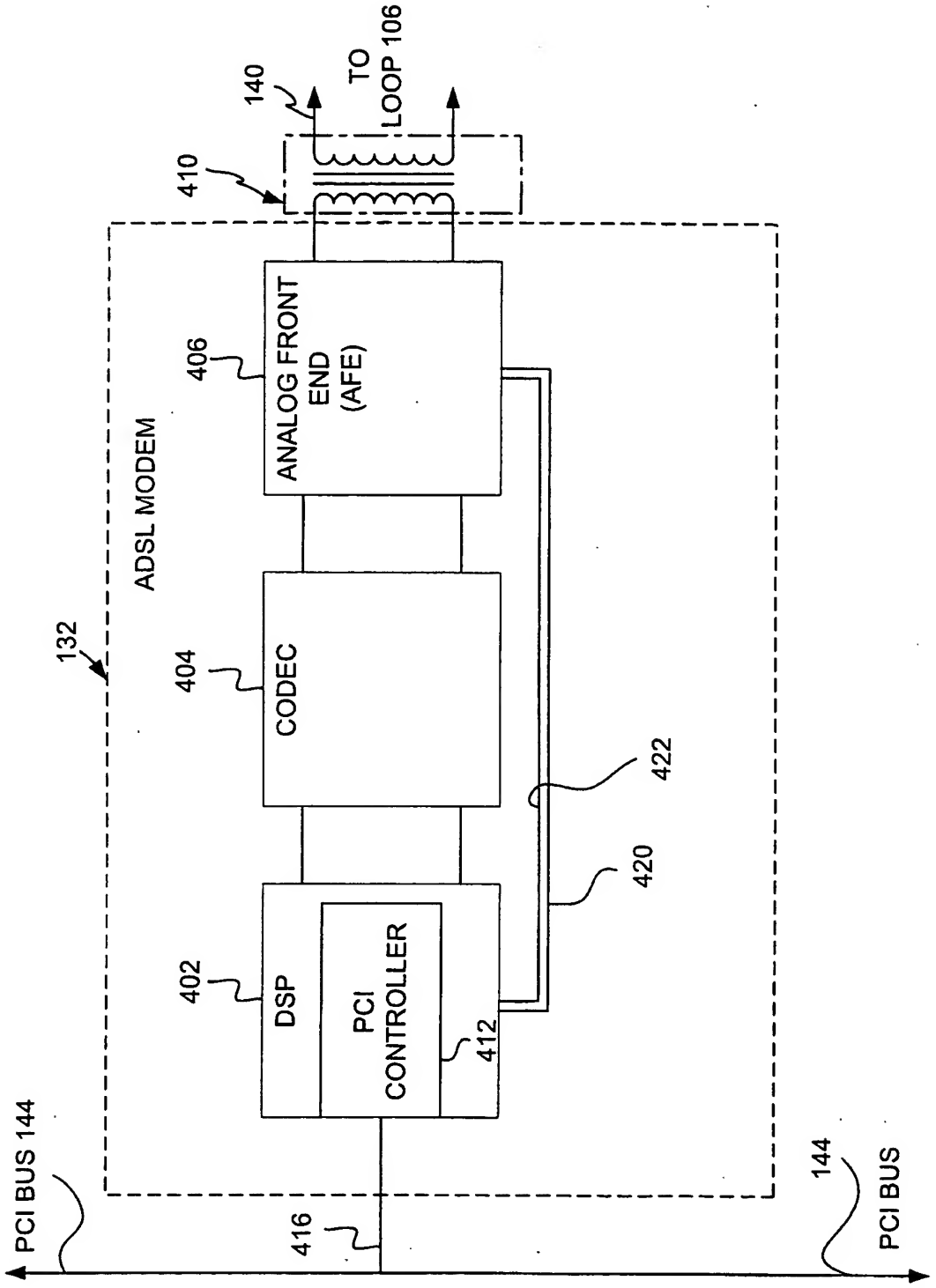
TO LOOP 106
140
410
ADSL MODEM
132
406
ANALOG FRONT END (AFE)
404
CODEC
422
420
402
DSP
PCI CONTROLLER
412
PCI BUS 144
416
144
PCI BUS

FIG. 4

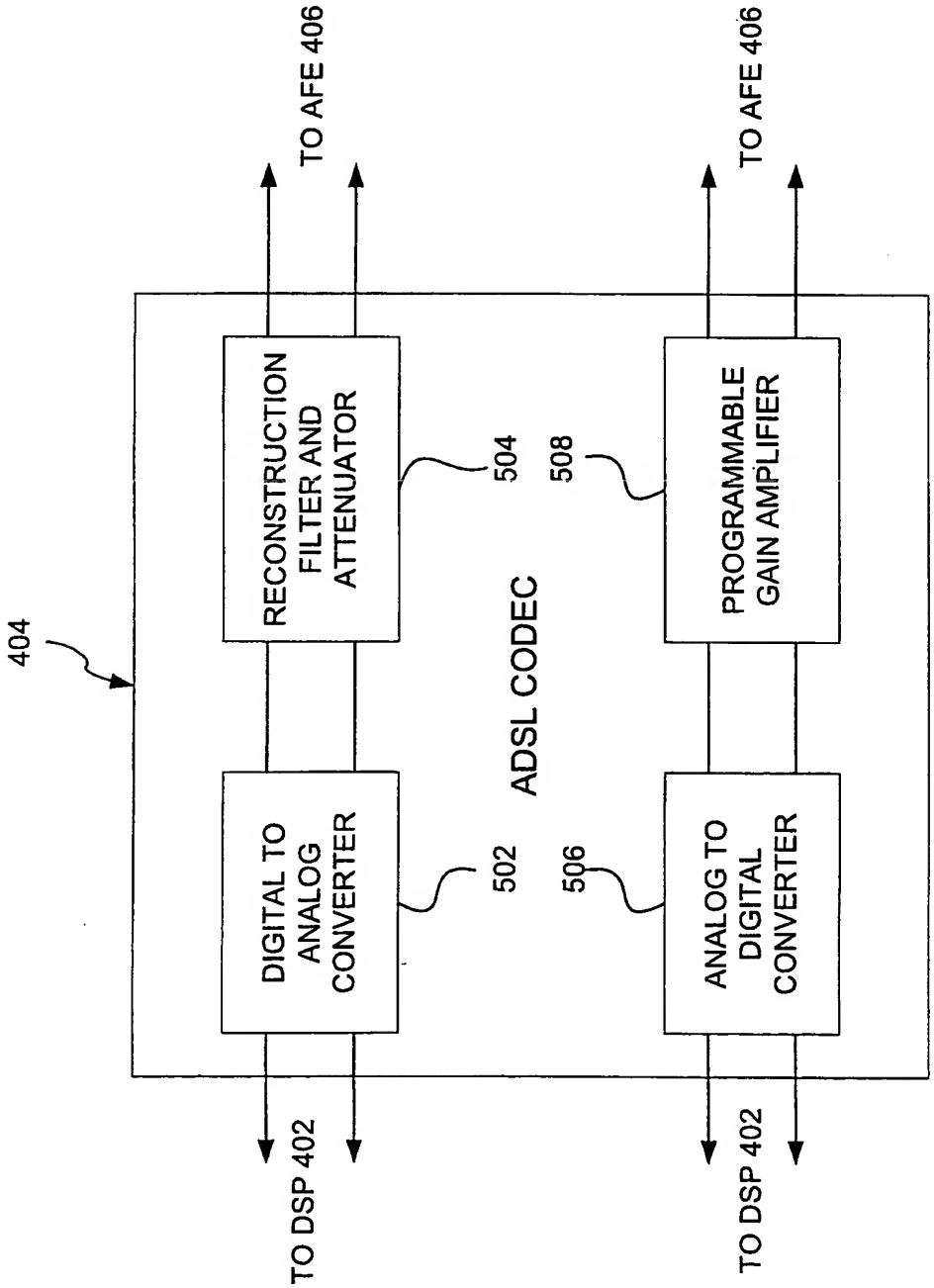
404
TO AFE 406
TO AFE 406
RECONSTRUCTION FILTER AND ATTENUATOR
504
508
PROGRAMMABLE GAIN AMPLIFIER
ADSL CODEC
DIGITAL TO ANALOG CONVERTER
502
506
ANALOG TO DIGITAL CONVERTER
TO DSP 402
TO DSP 402

FIG. 5

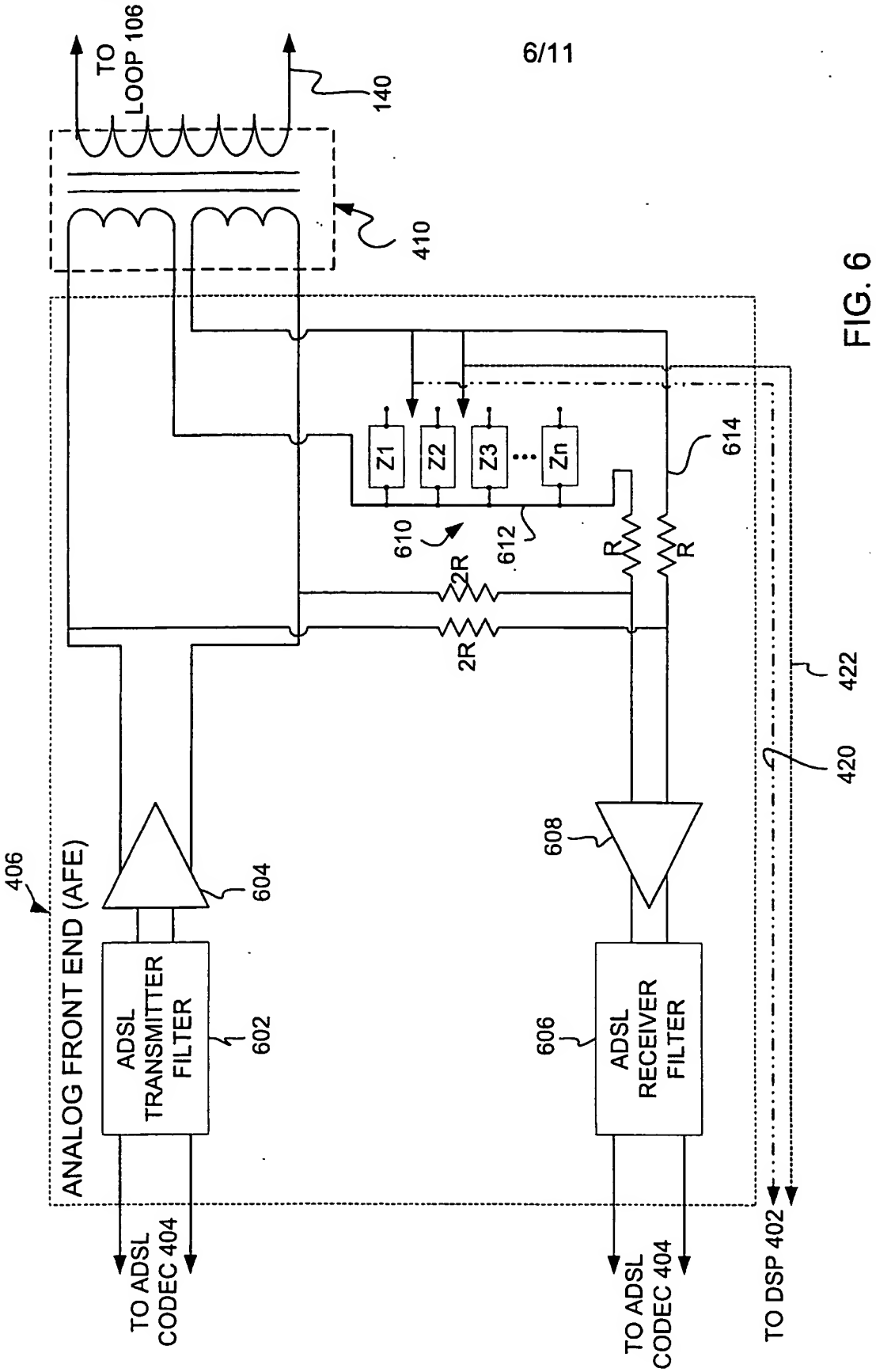
TO LOOP 106
140
410
Z1
Z2
Z3
Zn
614
610
612
R
R
2R
2R
422
420
406
ANALOG FRONT END (AFE)
604
608
ADSL TRANSMITTER FILTER
602
606
ADSL RECEIVER FILTER
TO ADSL CODEC 404
TO ADSL CODEC 404
TO DSP 402

FIG. 6

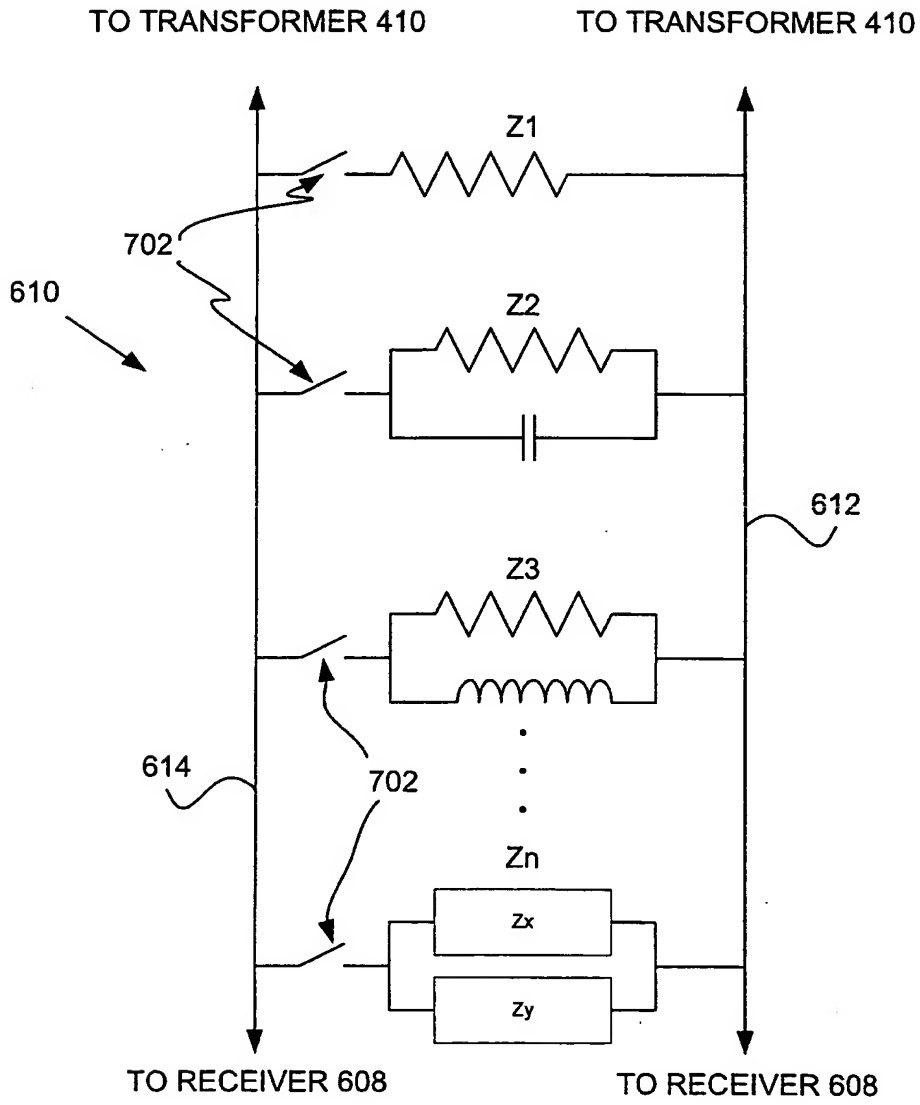
TO TRANSFORMER 410
TO TRANSFORMER 410
Z1
702
610
Z2
612
Z3
614
702
Zn
Zx
Zy
TO RECEIVER 608
TO RECEIVER 608

FIG. 7A

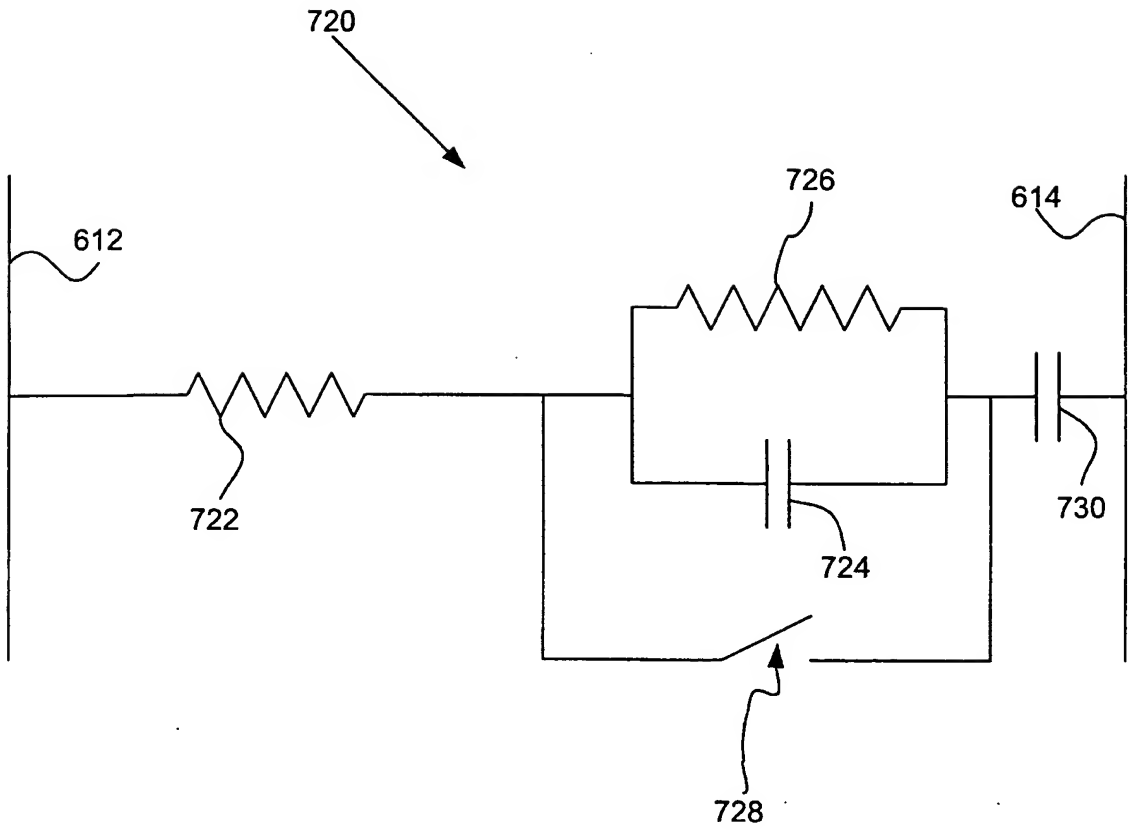

FIG. 7B

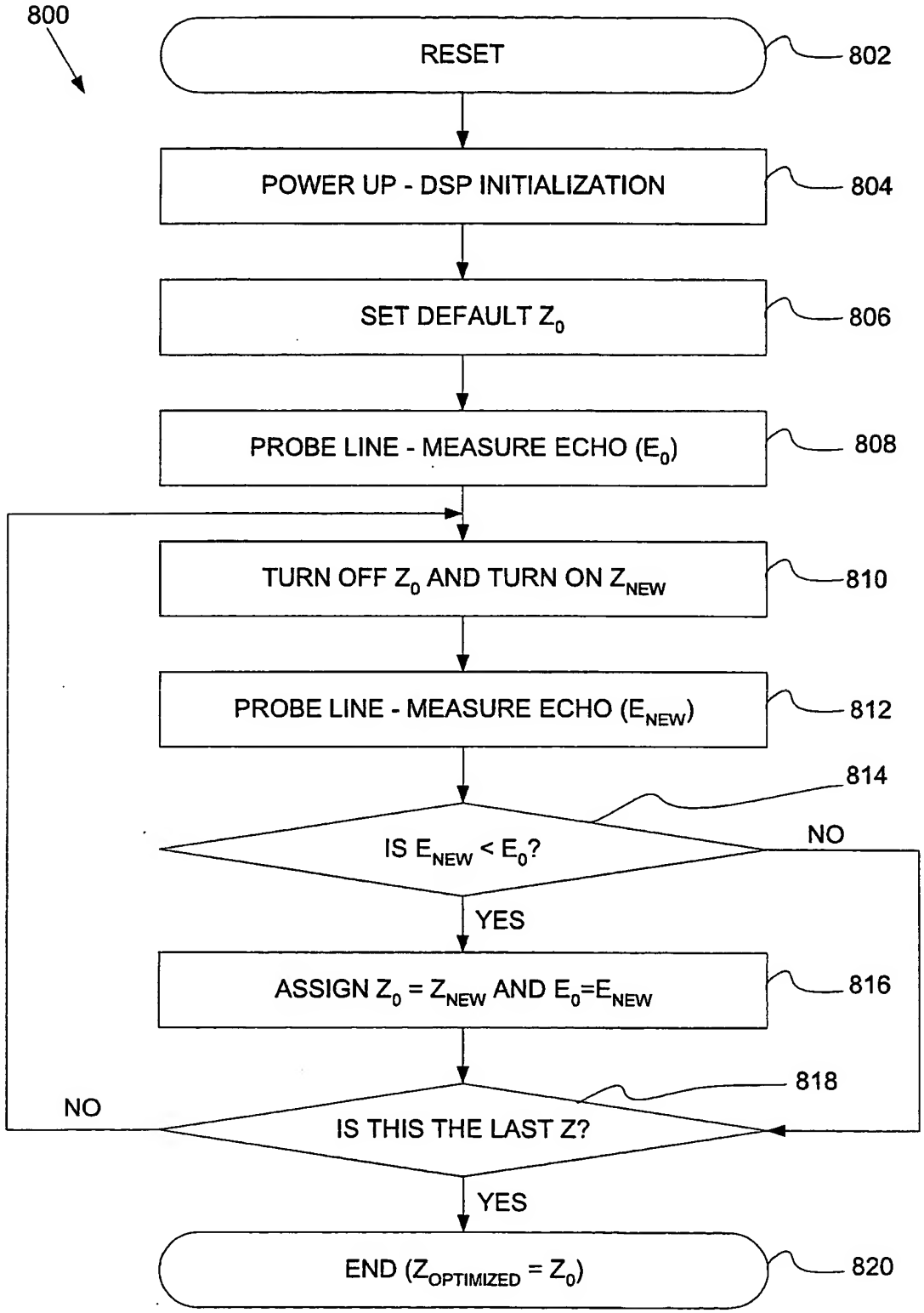
800
RESET
802
POWER UP - DSP INITIALIZATION
804
SET DEFAULT Z_0
806
PROBE LINE - MEASURE ECHO (E_0)
808
TURN OFF Z_0 AND TURN ON Z_{NEW}
810
PROBE LINE - MEASURE ECHO (E_{NEW})
812
814
IS $E_{NEW} < E_0$?
NO
YES
ASSIGN $Z_0 = Z_{NEW}$ AND $E_0 = E_{NEW}$
816
818
NO
IS THIS THE LAST Z?
YES
END ($Z_{OPTIMIZED} = Z_0$)
820

FIG. 8

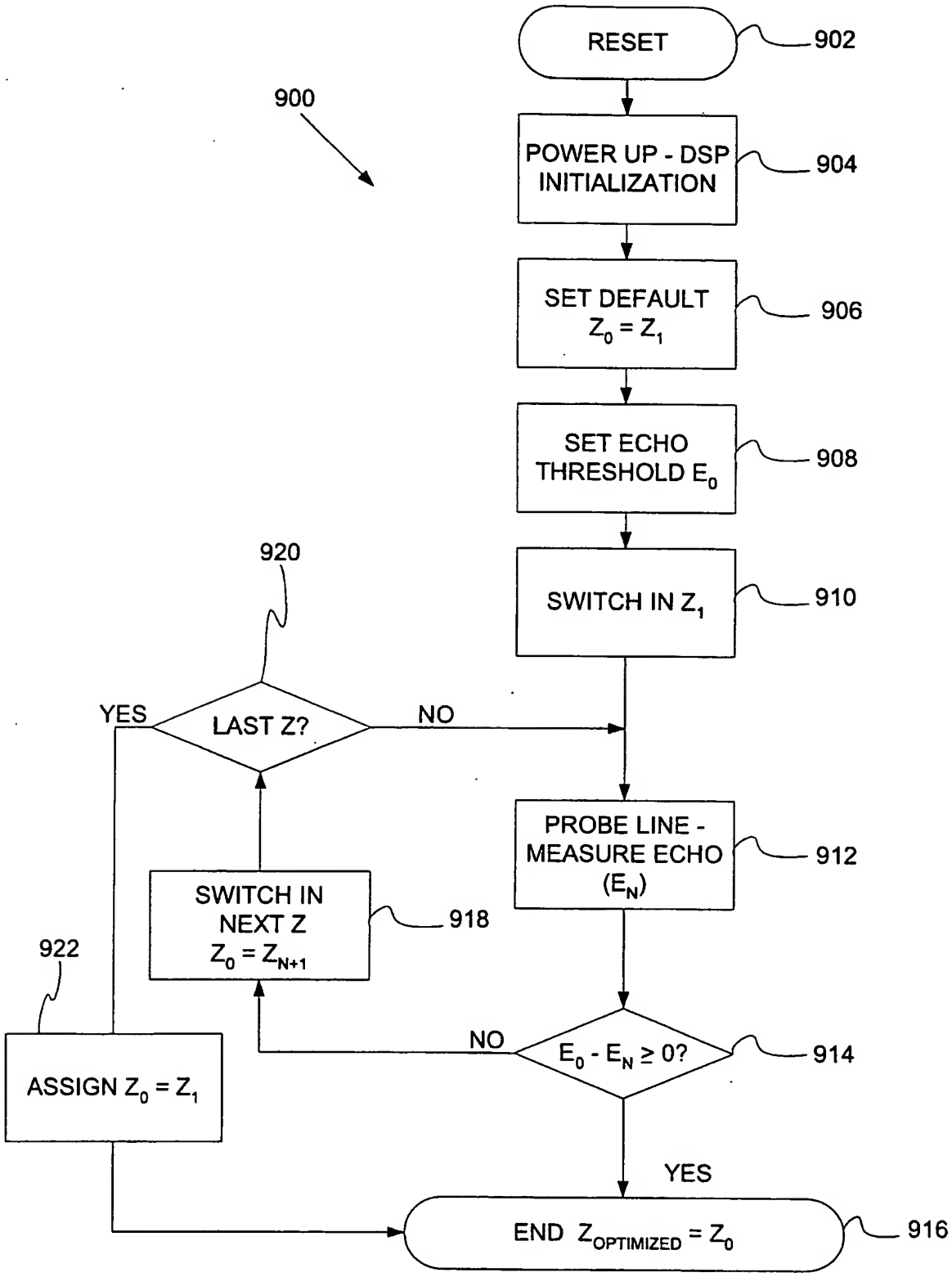
RESET
902
900
POWER UP - DSP INITIALIZATION
904
SET DEFAULT $Z_0 = Z_1$
906
SET ECHO THRESHOLD E_0
908
920
SWITCH IN Z_1
910
YES
LAST Z?
NO
PROBE LINE - MEASURE ECHO (E_N)
912
SWITCH IN NEXT Z $Z_0 = Z_{N+1}$
918
922
NO
$E_0 - E_N \geq 0$?
914
ASSIGN $Z_0 = Z_1$
YES
END $Z_{OPTIMIZED} = Z_0$
916

FIG. 9

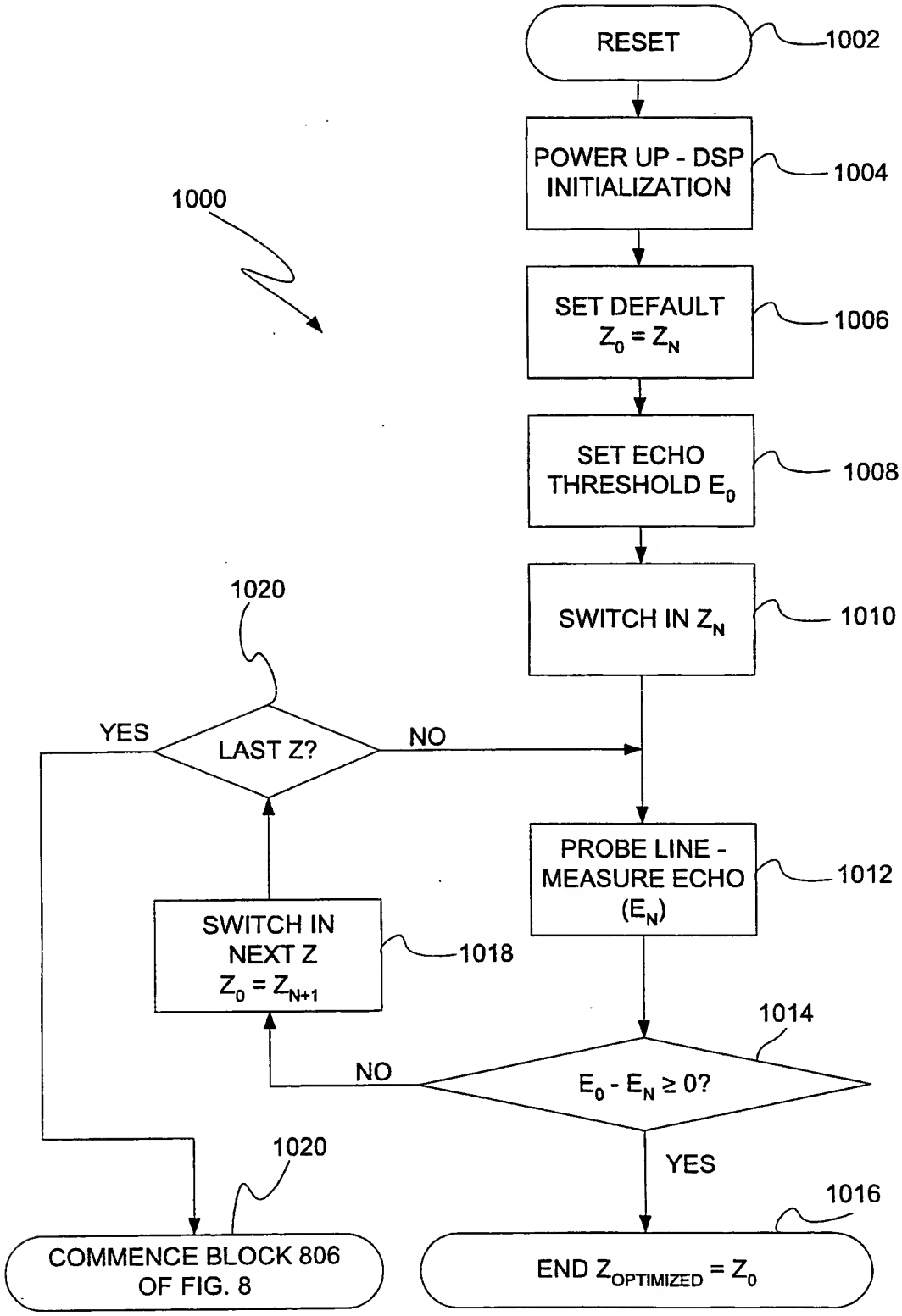
RESET
1002
POWER UP - DSP INITIALIZATION
1004
1000
SET DEFAULT $Z_0 = Z_N$
1006
SET ECHO THRESHOLD E_0
1008
1020
SWITCH IN Z_N
1010
YES
LAST Z?
NO
PROBE LINE - MEASURE ECHO (E_N)
1012
SWITCH IN NEXT Z $Z_0 = Z_{N+1}$
1018
1014
NO
$E_0 - E_N \geq 0$?
1020
YES
1016
COMMENCE BLOCK 806 OF FIG. 8
END $Z_{OPTIMIZED} = Z_0$

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/40226

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04B 1/38, 1/58; H04M 7/04
US CL : 379/398, 399, 400, 402, 403, 404; 375/222

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 379/398, 399, 400, 402, 403, 404; 375/222

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,187,742 A (MORAN III et al) 16 FEBRUARY 1993, figures 3-12; col. 1, lines 6-12; col. 3, lines 23-67; col. 4, lines 1-67; col. 5, lines 1-65; col. 7, lines 3-67; col. 8, lines 1-10	1-30
Y	US 5,802,169 A (FRANTZ et al) 01 SEPTEMBER 1998, figures 1-6; col. 2, lines 40-67; col. 3, lines 1-64;	1, 2, 8-12, 15, 16, 19, 20,22-24, 26-30
Y	US 5,386,438 A (ENGLAND) 31 JANUARY 1995, figures 1-3; col. 3, lines 4-29; col. 5, lines 64-67; col. 6, lines 1-66;	1, 3,14, 25
Y	US 5,400,394 A (RAMAN et al) 21 MARCH 1995, figures 3-5; appendix-A.	5, 18, 30
Y	US 5,353,334 A (O'SULLIVAN) 04 OCTOBER 1994, figures 1, 8; col. 3, lines 30-43; col. 4, lines 17-27; col. 12, lines 65-67; col. 13, lines 1-39; col. 14, lines 63-67; col. 15, lines 1-66; col. 16, lines 6-13; col. 35, lines 30-55.	1, 20
Y,P	US 5,953,412 A (SHEETS et al) 14 SEPTEMBER 1999, figures 9-12. col. 7, lines 42-67; col. 8, lines 1-9; col. 15, lines 5-22.	6, 17
Y,P	US 6,044,107 A (GATHERER et al) 28 MARCH 2000, entire patent.	1-4, 6, 7, 13, 21, 25, 27, 30

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 OCTOBER 2000	04 DEC 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Forester Isen Telephone No. (703)305-9900

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/40226

Continuation of B. FIELDS SEARCHED Item3: Us Patents Full-Text Database ; JPO Abstracts Database
EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins
Search terms used; ADSL modem, modem ineterfacing computer, analog front end, hybrid impedance matching, dynamic impedance matching, echo threshold, minimum echo signal